AMENDMENTS TO THE CLAIMS:

This listing of claims will replace all prior versions, and listings, of claims in the application:

LISTING OF CLAIMS:

1. (Cancelled)

2. (Currently Amended) A data processor comprising:

a status register;

a central processing unit including a predetermined register set; and

a plurality of register banks corresponding to the predetermined register set,

wherein the status register includes an overflow flag to indicate an overflow of the plurality of register banks,

wherein the central processing unit operates to store information from the predetermined register set to one of the plurality of register banks when an interrupt occurs and the overflow flag indicates non-occurrence of the overflow of the plurality of register banks, and

wherein the central processing unit operates to store information from the predetermined register set to a stack area when an interrupt occurs and the overflow flag

indicates occurrence of the overflow of the plurality of register banks.

3. (Previously Presented) The data processor according to claim 2,

wherein, when an interrupt exception occurs in a state in which data has been saved to all banks of the register banks, and an accepted interrupt exception is permitted to use the register banks, the central processing unit saves data of the register set to a stack area and reflects an overflow state in the overflow flag.

4. (Original) The data processor according to claim 3,

wherein, when the overflow flag indicates an overflow state, if data restoration from the register banks to the register set is directed, the central processing unit restores the data from the stack area to the register set.

5. (Previously Presented) The data processor according to claim 2,

wherein, when an interrupt exception occurs in a state in which data has been saved to all banks of the register banks, and an accepted interrupt exception is permitted to use the register banks and specified to execute a

predetermined exception handling routine, the central processing unit executes the predetermined exception handling routine and does not perform saving to the register banks.

6. (Currently Amended) The data processor according to claim 2, comprising:

a memory having the plurality of register banks; and

a bus dedicated to couple the memory and the predetermined register set,

wherein the bus has a plurality of bit lines which are operable to transfer data from a plurality of registers of the register set~~includes as many bits as parallel data transfer is allowed in units of plural registers contained in the register set~~.

7. (Currently Amended) The data processor according to claim 2,

wherein the central processing unit, in response to the occurrence of an interrupt exception, saves information from the status register and a program counter to ~~a~~ the stack area, and saves information from the predetermined register set to the register banks.

8. (Currently Amended) The data processor according to claim 7,

wherein an operation to save to the register banks can be selected according to factors indicating types of interrupts or priority levels.

9. (Currently Amended) The data processor according to claim 7, which processes~~including~~ interrupts to ~~always~~ perform saving to the register banks and interrupts capable of ~~automatically~~ selecting a stack area as a save location when the number of remaining banks is ~~small~~smaller than the number of remaining interrupts to perform saving to the register banks.

10. (Original) The data processor according to claim 7,

wherein the central processing unit includes in an instruction set a register restore instruction to restore storage information from a register bank last saved to the predetermined register set.

11. (Original) The data processor according to claim 10,

wherein, if the register restore instruction is executed when the register banks are empty, predetermined exception service occurs.

12. (Original) The data processor according to claim 10,

wherein the instruction set includes a return instruction to restore a value of the program counter and a value of the status register stored in a stack area in interrupt exception handling and enable return to previous program execution processing.

Claims 13-15 (Cancelled)